UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,802	09/12/2003	Thomas D. Lovett	BEA920020019US1	8363

49474 7590 10/07/2008

LAW OFFICES OF MICHAEL DRYJA
1474 N COOPER RD #105-248
GILBERT, AZ 85233

EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
10/07/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,802	LOVETT ET AL.	
	Examiner	Art Unit	
	MIDYS ROJAS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/16/08 has been entered.

Response to Arguments

2. Applicant's arguments, filed on 8/16/2008, with respect to the rejection(s) of claim(s) 1 under 35 USC 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Palanca et al. (6,223,258).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams, III (2003/0110356 A1) in view of Palanca et al. (6,223,258).

Regarding Claim 1, Williams III discloses a method comprising:

evicting a first memory line currently stored in a cache (selecting a victim cache line to be replaced, paragraph 0035; if the cache line to replaced has been altered, it must be written back to main memory 8, paragraph 0036. The selection of the victim cache line and writing back to main memory if altered, represents the eviction of this cache line) and storing a second memory line not currently stored in the cache in place of the first memory line in the cache (when the processor executes an instruction that causes a cache miss, a line fill operation retrieves data from the main memory, selects a victim cache line to replace with this data and writes the new data in the victim cache line, paragraph 0035);

while evicting the first memory line, temporarily storing the second memory line in a buffer (fill buffer 12); a buffer also storing eviction data regarding the first memory line (evicted data is written to the write buffer 14, paragraph 0036) and data resulting from conversion of the second memory line into a set of concurrently performable actions (set of performable actions that follow for the completion of a line fill operation, paragraphs 0042-0049);

upon eviction of the first memory line, moving the second memory line from the buffer into the cache (paragraphs 0041-0049 describe the eviction of the victim cache line and the storage of the new cache line from the fill buffer to the location of the victim cache line).

Williams, III does not teach that the eviction data is stored in the same buffer as the second memory line wherein the eviction data is stored in only the buffer so that the eviction data is never stored in any other buffer other than the buffer.

Palanca et al. discloses the use of a load buffer to store read instructions and a write buffer to store write instructions (Col. 3, line 64- Col. 4, line 5). Palanca et al. also discloses that alternatively, the system may use a single unified buffer for storing both the read and write instructions. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Williams III (as shown in Figure 1) by replacing the two buffers 12 and 14 with an unified buffer as suggested by Palanca et al. since a unified buffer would provide for a simpler system with less components while also making the system more versatile by employing a buffer that has more than one use. Also, in employing one buffer instead of two, the modification would result in a cheaper system to manufacture.

Regarding Claim 2, Williams III in view of Palanca et al. discloses the method further initially comprising receiving a transaction relating to the second memory line not currently in the cache (load requests to data not residing in the cache resulting in load data access misses, paragraph 0035; servicing write requests, paragraph 0041).

Regarding Claim 3, Williams III in view of Palanca discloses the method further comprising, after temporarily storing the second memory line in the buffer, providing a response indicating that a transaction relating to the second memory line has been performed (data word that gave rise to the miss is recovered form main memory and streamed to the cache, stored in the fill buffer, and streamed in parallel to the requesting processor; paragraphs 0037 and 0041; wherein the response to the request indicating that the transaction has been performed is in the form of servicing the request by streaming the data to the requesting processor).

Regarding Claim 4, Williams III in view of Palanca discloses the method wherein evicting the first memory line currently stored in the cache comprises inserting the first memory line in an eviction queue of memory lines to be evicted from the cache (dirty data to be evicted is written out to a write buffer and then written to the main memory, paragraph 0036 wherein the write buffer represents the eviction queue since it holds that data will be evicted once it is replaced by the new cache line).

Regarding Claim 5, Williams III in view of Palanca discloses the method wherein temporarily storing the second memory line in the buffer comprises temporarily storing the second memory line in a data transfer buffer (DTB). The new data that is to be written to the cache (data the caused the cache miss) is written to a fill buffer 12 wherein the fill buffer is a DTB since it buffers the data that is being transferred from the main memory to the cache (paragraph 0041).

5. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams III (2003/0110356 A1) in view of Palanca et al. (6,223,258) further in view of Chryson et al. (6,549,930).

Regarding Claim 6, Williams III in view of Palanca et al. discloses the method of Claim 1 above. Williams III in view of Palanca et al. does not teach converting a transaction to which the second memory line relates into a set of concurrently performable actions using a multiple-stage pipeline.

Chryson et al. discloses converting a transaction (in the pipeline the instructions are decoded for execution, Col. 8, lines 51-55) into a set of concurrently performable actions (plurality of stages serially arranged such as fetch, map, issue, execute, and

retire, Col. 8, lines 62-64) using a multiple-stage pipeline (multiple execution pipeline, Col. 8, lines 34-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Williams III in view of Palanca et al. to include the multiple stage pipeline of Chryson since the multiple stages of the pipeline allow improved system performance.

Regarding Claim 7, Williams III in view of Palanca et al. further in view of Chryson et al. discloses the method wherein evicting the first memory line currently stored in the cache comprises inserting the first memory line in an eviction queue of memory lines to be evicted from the cache (dirty data to be evicted is written out to a write buffer and then written to the main memory, paragraph 0036) after the transaction has been converted into the set of concurrently performable actions (since a transaction causes the cache miss, which in turn caused the eviction, then the transaction must have been converted in order to be executed) .

Regarding Claim 8, Williams III in view of Palanca et al. further in view of Chryson et al. discloses the method wherein temporarily storing the second memory line in the buffer comprises temporarily storing the second memory line in a data transfer buffer (DTB). The new data that is to be written to the cache (data the caused the cache miss) is written to a fill buffer 12 wherein the fill buffer is a DTB since it buffers the data that is being transferred from the main memory to the cache (paragraph 0041).

Regarding Claim 9, Williams III in view of Palanca et al. further in view of Chryson et al. discloses the method further comprising, after temporarily storing the second memory line in the buffer, providing a response indicating that a transaction

relating to the second memory line has been performed (data word that gave rise to the miss is recovered form main memory and streamed to the cache, stored in the fill buffer, and streamed in parallel to the requesting processor; paragraphs 0037 and 0041; wherein the response to the request indicating that the transaction has been performed is in the form of servicing the request by streaming the data to the requesting processor).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Midys Rojas/
Examiner, Art Unit 2185

MR